

08/876,414

(FILE 'USPAT' ENTERED AT 08:35:12 ON 22 JUL 1998)

L1 38 S GILD

L2 16 S L1(P)DOP##

=> d cit ab 12 1-

1. 5,688,715, Nov. 18, 1997, Excimer laser dopant activation of backside illuminated CCD's; Douglas A. Sexton, et al., 438/75; 148/DIG.90; 438/144, 308, 530, 795 [IMAGE AVAILABLE]

US PAT NO: 5,688,715 [IMAGE AVAILABLE]

L2: 1 of 16

**ABSTRACT:**

A method uses an excimer laser to activate previously implanted dopant species in the backside of a backside-illuminated CCD or to incorporate dopant ions from a gaseous ambient into the backside of a backside-illuminated CCD and simultaneously activate. The controlled ion implantation of the backside and subsequent thin layer heating by the short wavelength pulsed excimer laser energy activates the dopant and provides for an improved dark current response and improved spectral response. The energy of the pulsed excimer laser is applied uniformly across a backside-illuminated CCD in a very thin layer of the semiconductor substrate (usually silicon) material that requires annealing to uniformly activate the dopant. The very thin layer of the material can be heated to exceedingly high temperatures on a nanosecond time scale while the bulk of the delicate CCD substrate remains at low temperature. Repair of semiconductor dies by effecting a uniform annealing enables salvage and utilization of otherwise discardable components by bringing their dark current response to within an acceptable range.

2. H 1,637, Mar. 4, 1997, Laser-assisted fabrication of bipolar transistors in silicon-on-sapphire (SOS); Bruce W. Offord, et al., 438/311; 148/DIG.11, DIG.92, DIG.150; 438/799 [IMAGE AVAILABLE]

US PAT NO: H 1,637 [IMAGE AVAILABLE]

L2: 2 of 16

**ABSTRACT:**

The fabrication of bipolar junction transistors in silicon-on-sapphire (SOS) relies upon the laser-assisted dopant activation in SOS. A patterned 100% aluminum mask whose function is to reflect laser light from regions where melting of the silicon is undesirable is provided on an SOS wafer to be processed. The wafer is placed within a wafer carrier that is evacuated and backfilled with an inert atmosphere and that is provided with a window transparent to the wavelength of the laser beam to allow illumination of the masked wafer when the carrier is inserted into a laser processing system. A pulsed laser (typically an excimer laser) beam is appropriately shaped and homogenized and one or more pulses are directed onto the wafer. The laser beam pulse energy and pulse duration are set to obtain the optimal fluence impinging on the wafer in order to achieve the desired melt duration and corresponding junction depth. Care must be taken since activation and rapid dopant redistribution occurs when the laser fluence is above the melt threshold and below the ablation threshold. Thus, bipolar junction transistors in SOS utilize a pulsed laser activation of ion implanted dopant atoms. Appropriate masking and pulsed laser illumination assures the electrical activation of the dopant without allowing undesirable diffusion either vertically along crystallographic defects (diffusion pipes) or laterally.

3. 5,599,734, Feb. 4, 1997, Method for fabricating MOS transistor utilizing doped disposable layer; Jeong S. Byun, et al., 438/143; 148/DIG.144; 438/301, 563 [IMAGE AVAILABLE]

**ABSTRACT:**

A method for fabricating an MOS transistor includes the steps of forming a gate insulating layer on a substrate of a first conductivity-type, forming a gate on the gate insulating layer, forming a disposable layer over an entire surface of the substrate and the gate, the disposable layer having a first conductivity-type impurity and a second conductivity-type impurity of a higher concentration than that of the first conductivity-type impurity, and forming a source and drain area of the second conductivity-type impurity on the substrate by diffusing the second conductivity-type impurity of the disposable layer into the substrate by means of an annealing process, wherein the disposable layer includes a BPSG layer, wherein the BPSG layer is a B+PSG layer which is doped with a higher dopant concentration of boron than that of phosphorus to make a p-type MOS transistor.

4. 5,591,667, Jan. 7, 1997, Method for fabricating MOS transistor utilizing doped disposable layer; Jeong S. Byun, et al., 438/301, 143, 563 [IMAGE AVAILABLE]

US PAT NO: 5,591,667 [IMAGE AVAILABLE]

L2: 4 of 16

**ABSTRACT:**

A method for fabricating an MOS transistor includes the steps of forming a gate insulating layer on a substrate of a first conductivity-type, forming a gate on the gate insulating layer, forming a disposable layer over an entire surface of the substrate and the gate, the disposable layer having a first conductivity-type impurity and a second conductivity-type impurity of a higher concentration than that of the first conductivity-type impurity, and forming a source and drain area of the second conductivity-type impurity on the substrate by diffusing the second conductivity-type impurity of the disposable layer into the substrate by means of an annealing process, wherein the disposable layer includes a BPSG layer.

5. 5,569,624, Oct. 29, 1996, Method for shallow junction formation; Kurt H. Weiner, 438/285; 148/DIG.90; 438/301, 308, 559, 563, 923 [IMAGE AVAILABLE]

US PAT NO: 5,569,624 [IMAGE AVAILABLE]

L2: 5 of 16

**ABSTRACT:**

A doping sequence that reduces the cost and complexity of forming source/drain regions in complementary metal oxide silicon (CMOS) integrated circuit technologies. The process combines the use of patterned excimer laser annealing, dopant-saturated spin-on glass, silicide contact structures and interference effects creates by thin dielectric layers to produce source and drain junctions that are ultrashallow in depth but exhibit low sheet and contact resistance. The process utilizes no photolithography and can be achieved without the use of expensive vacuum equipment. The process margins are wide, and yield loss due to contact of the ultrashallow dopants is eliminated.

6. 5,550,082, Aug. 27, 1996, Method and apparatus for doping silicon wafers using a solid dopant source and rapid thermal processing; John C. Wolfe, et al., 438/567 [IMAGE AVAILABLE]

US PAT NO: 5,550,082 [IMAGE AVAILABLE]

L2: 6 of 16

**ABSTRACT:**

The present invention is, in part, a new process for dopant diffusion, both p-type (e.g., B) and n-type (e.g., P, As), into silicon wafers, using rapid thermal processing (RTP). It uses a surface layer of a new

planar dopant as an active dopant source. Such a source is produced using either a rigid holder wafer with a spin-on dopant or doped oxides deposited on its surface, or such a source is high pressure planar solid source having a surface that has been activated by dry etching or sputtering etching. Such a dopant source is placed in proximity to a processed silicon wafer in such a manner that its active surface is facing the surface of the silicon wafer during RTP. Both the silicon wafer and the dopant source are heated by lamps emitting light causing transport of dopant from the dopant source to the silicon surface. The dopant source may be produced using either silicon wafers, quartz or ceramic plates or planar solid diffusion sources which are commercially available in a form of solid discs containing compounds containing various dopant atoms (e.g., B, P, and As).

7. 5,471,330, Nov. 28, 1995, Polysilicon pixel electrode; Kalluri R. Sarma, 349/43; 257/59, 72; 349/140; 438/30, 158 [IMAGE AVAILABLE]

US PAT NO: 5,471,330 [IMAGE AVAILABLE]

L2: 7 of 16

**ABSTRACT:**

A liquid crystal display wherein each pixel has a thin film transistor with a silicon pixel electrode. A doping and recrystallization of the silicon is effected to increase the electrical conductivity and light transmittance of the silicon adequately for the pixel electrode.

8. 5,456,763, Oct. 10, 1995, Solar cells utilizing pulsed-energy crystallized microcrystalline/polycrystalline silicon; James L. Kaschmitter, et al., 136/258; 257/49, 75; 438/97, 487 [IMAGE AVAILABLE]

US PAT NO: 5,456,763 [IMAGE AVAILABLE]

L2: 8 of 16

**ABSTRACT:**

A process for producing multi-terminal devices such as solar cells wherein a pulsed high energy source is used to melt and crystallize amorphous silicon deposited on a substrate which is intolerant to high processing temperatures, whereby amorphous silicon is converted into a microcrystalline/polycrystalline phase. Dopant and hydrogenation can be added during the fabrication process which provides for fabrication of extremely planar, ultra shallow contacts which results in reduction of non-current collecting contact volume. The use of the pulsed energy beams results in the ability to fabricate high efficiency microcrystalline/polycrystalline solar cells on the so-called low-temperature, inexpensive plastic substrates which are intolerant to high processing temperatures.

9. 5,346,850, Sep. 13, 1994, Crystallization and doping of amorphous silicon on low temperature plastic; James L. Kaschmitter, et al., 438/487, 96, 535 [IMAGE AVAILABLE]

US PAT NO: 5,346,850 [IMAGE AVAILABLE]

L2: 9 of 16

**ABSTRACT:**

A method or process of crystallizing and doping amorphous silicon (a-Si) on a low-temperature plastic substrate using a short pulsed high energy source in a selected environment, without heat propagation and build-up in the substrate. The pulsed energy processing of the a-Si in a selected environment, such as BF<sub>3</sub> and PF<sub>5</sub>, will form a doped micro-crystalline or poly-crystalline silicon (pc-Si) region or junction point with improved mobilities, lifetimes and drift and diffusion lengths and with reduced resistivity. The advantage of this method or process is that it provides for high energy materials processing on low cost, low temperature, transparent plastic substrates. Using pulsed laser processing a high (>900. degree. C.), localized processing temperature can be achieved in thin films, with little accompanying temperature rise in the substrate, since substrate temperatures do not exceed 180. degree. C. for more than a

few microseconds. The method enables use of plastics incapable of withstanding sustained processing temperatures (higher than 180. degree. C.) but which are much lower cost, have high tolerance to ultraviolet light, have high strength and good transparency, compared to higher temperature plastics such as polyimide.

10. 5,323,013, Jun. 21, 1994, Method of rapid sample handling for laser processing; Eugene P. Kelly, et al., 250/522.1; 422/186.3 [IMAGE AVAILABLE]

US PAT NO: 5,323,013 [IMAGE AVAILABLE]

L2: 10 of 16

**ABSTRACT:**

A method of rapid sample handling in a production environment for laser processing of individual microelectronic die is particularly suited for handling partially fabricated die and die which are susceptible to mechanical and electrostatic damage, such as backside illuminated CCDs requiring backside dopant activation and laser texturing of sidewalls. Securing a die within a modified sample holder provides for electrostatic and mechanical protection during laser processing. Placing the modified die holder onto a feeder base portion that engages a "tractor-feed" translation subsystem protects the die during a translation and positioning of the die below and aligned with a laser processing structure. A window holder is engaged with the die holder to seal the die in a processing chamber and to assure an appropriate pressurizing with a gaseous ambient for a desired processing. Illuminating, repetitively if desired, the die in the chamber with a laser beam of appropriate size, laser fluence, repetition rate and number of pulses processes the die. Next, the processed die is translated from beneath laser processing structure while the next die is correctly positioned for processing.

11. 5,316,969, May 31, 1994, Method of shallow junction formation in semiconductor devices using gas immersion laser doping; Emi Ishida, et al., 438/535; 148/DIG.129 [IMAGE AVAILABLE]

US PAT NO: 5,316,969 [IMAGE AVAILABLE]

L2: 11 of 16

**ABSTRACT:**

Shallow regions are formed in a semiconductor body by irradiating the surface region with a pulsed laser beam in an atmosphere including the dopant. The pulsed laser beam has sufficient intensity to drive in dopant atoms from the atmosphere but insufficient intensity to melt the semiconductor material. A silicide layer can be placed over the surface of the semiconductor material prior to irradiation with the dopant being driven from the atmosphere through the silicide into the surface region of the semiconductor body. Alternatively, the silicide layer can include dopant atoms prior to irradiating the surface region.

12. 5,250,452, Oct. 5, 1993, Deposition of germanium thin films on silicon dioxide employing interposed polysilicon layer; Mehmet Ozturk, et al., 438/301; 148/DIG.59, DIG.105; 438/592 [IMAGE AVAILABLE]

US PAT NO: 5,250,452 [IMAGE AVAILABLE]

L2: 12 of 16

**ABSTRACT:**

The invention is a method of depositing a layer of polycrystalline silicon on a silicon dioxide substrate until the layer of polycrystalline silicon is thick enough to support the deposition of germanium thereon, but while thin enough to substantially avoid the deleterious effects on the characteristics of semiconductor device structure that the deposition of polycrystalline silicon would otherwise potentially cause. The polycrystalline layer is then exposed to a germanium containing gas at a temperature below the temperature at which germanium will deposit on silicon dioxide alone while preventing native growth of silicon dioxide on the polycrystalline silicon layer, and for a time sufficient for a

desired thickness of polycrystalline germanium to be deposited on the layer of polycrystalline silicon.

13. 5,114,876, May 19, 1992, Selective epitaxy using the gild process; Kurt H. Weiner, 117/53, 58; 148/DIG.105, DIG.106; 438/498, 535 [IMAGE AVAILABLE]

US PAT NO: 5,114,876 [IMAGE AVAILABLE]

L2: 13 of 16

**ABSTRACT:**

The present invention comprises a method of selective epitaxy on a semiconductor substrate. The present invention provides a method of selectively forming high quality, thin GeSi layers in a silicon circuit, and a method for fabricating smaller semiconductor chips with a greater yield (more error free chips) at a lower cost. The method comprises forming an upper layer over a substrate, and depositing a reflectivity mask which is then removed over selected sections. Using a laser to melt the unmasked sections of the upper layer, the semiconductor material in the upper layer is heated and diffused into the substrate semiconductor material. By varying the amount of laser radiation, the epitaxial layer is formed to a controlled depth which may be very thin. When cooled, a single crystal epitaxial layer is formed over the patterned substrate. The present invention provides the ability to selectively grow layers of mixed semiconductors over patterned substrates such as a layer of Ge<sub>sub.x</sub> Si<sub>sub.1-x</sub> grown over silicon. Such a process may be used to manufacture small transistors that have a narrow base, heavy doping, and high gain. The narrowness allows a faster transistor, and the heavy doping reduces the resistance of the narrow layer. The process does not require high temperature annealing; therefore materials such as aluminum can be used. Furthermore, the process may be used to fabricate diodes that have a high reverse breakdown voltage and a low reverse leakage current.

14. 5,101,247, Mar. 31, 1992, Germanium silicon dioxide gate MOSFET; Mehmet Ozturk, et al., 257/410, 288, 411, 412 [IMAGE AVAILABLE]

US PAT NO: 5,101,247 [IMAGE AVAILABLE]

L2: 14 of 16

**ABSTRACT:**

The invention is a method of depositing a layer of polycrystalline silicon on a silicon dioxide substrate until the layer of polycrystalline silicon is thick enough to support the deposition of germanium thereon, but while thin enough to substantially avoid the deleterious effects on the characteristics of semiconductor device structure that the deposition of polycrystalline silicon would otherwise potentially cause. The polycrystalline layer is then exposed to a germanium containing gas at a temperature below the temperature at which germanium will deposit on silicon dioxide alone while preventing native growth of silicon dioxide on the polycrystalline silicon layer, and for a time sufficient for a desired thickness of polycrystalline germanium to be deposited on the layer of polycrystalline silicon.

15. 4,932,747, Jun. 12, 1990, Fiber bundle homogenizer and method utilizing same; Stephen D. Russell, et al., 385/115; 65/410; 219/121.6, 121.61, 121.79; 362/32, 259; 372/57; 385/121 [IMAGE AVAILABLE]

US PAT NO: 4,932,747 [IMAGE AVAILABLE]

L2: 15 of 16

**ABSTRACT:**

An apparatus and method are provided to homogenize the intensity profile of the beam emitted by an excimer laser. The excimer laser beam is collected by a closely packed ultraviolet-grade optical fiber bundle array having its individual fibers intermingled in a random or preconceived format to result in an intermixing of the light from the individual fiber cores to produce a uniform intensity profile. The output

ends of the fibers are gathered or fused, and optionally tapered, before being cleaved to provide an output face that is custom shaped for a desired illumination pattern. The flexible nature of the fiber bundle allows for remote materials processing applications.

16. 4,350,990, Sep. 21, 1982, Electrode for lead-salt diodes; Wayne Lo, 372/44; 257/188, 613, 744, 772; 438/569, 602 [IMAGE AVAILABLE]

US PAT NO: 4,350,990 [IMAGE AVAILABLE]

L2: 16 of 16

ABSTRACT:

A significantly more stable ohmic contact for a lead-salt semiconductor surface, especially for use in infrared lasers. The contact has layers of platinum, palladium or nickel alternating with gold, and then covered with indium. An Au-Pd-Au-In contact is used on lead-sulfide-selenide, lead-tin-selenide, and lead-tin-telluride of high tin content. A Pt-Au-Pt-Sn contact is preferred for lead-tin-telluride of low tin content. Lower contact resistance is attained if P type lead-tin-selenide and lead-tin-telluride surfaces are previously doped with oxygen, and the initial metal layer is applied in a manner that does not remove it.

(FILE 'USPAT' ENTERED AT 08:35:12 ON 22 JUL 1998)

L1 38 S GILD

L2 16 S L1(P)DOP##

08/876,414

(FILE 'USPAT' ENTERED AT 08:35:12 ON 22 JUL 1998)

L1 65490 S DOP##  
L2 278457 S PULS####  
L3 11195 S L1 AND L2  
L4 1841 S ELECTRICALLY ACTIVE  
L5 101 S L3 AND L4

=> d cit 15 1-

1. 5,781,670, Jul. 14, 1998, Optical frequency channel selection filter with electronically-controlled grating structures; David A. G. Deacon, et al., 385/10; 359/326, 573; 385/15, 37, 40 [IMAGE AVAILABLE]
2. 5,766,697, Jun. 16, 1998, Method of making ferroelectric thin film composites; Somnath Sengupta, et al., 427/585, 255.3, 596 [IMAGE AVAILABLE]
3. 5,751,422, May 12, 1998, In-situ particle detection utilizing optical coupling; John R. Mitchell, 356/337 [IMAGE AVAILABLE]
4. 5,732,177, Mar. 24, 1998, Controllable beam director using poled structure; David A. G. Deacon, et al., 385/122, 8, 37, 129 [IMAGE AVAILABLE]
5. 5,724,463, Mar. 3, 1998, Projection display with electrically controlled waveguide-routing; David A. G. Deacon, et al., 385/27, 9, 10, 18, 47, 901 [IMAGE AVAILABLE]
6. 5,719,410, Feb. 17, 1998, Semiconductor device wiring or electrode; Shintaro Suehiro, et al., 257/77, 750, 754, 768, 770 [IMAGE AVAILABLE]
7. 5,703,710, Dec. 30, 1997, Method for manipulating optical energy using poled structure; Michael J. Brinkman, et al., 359/283, 251, 252 [IMAGE AVAILABLE]
8. 5,696,392, Dec. 9, 1997, Barrier layers for oxide superconductor devices and circuits; Kookrin Char, et al., 257/190, 31, 33, 35; 505/238, 329, 702, 781 [IMAGE AVAILABLE]
9. 5,688,715, Nov. 18, 1997, Excimer laser **dopant** activation of backside illuminated CCD's; Douglas A. Sexton, et al., 438/75; 148/DIG.90; 438/144, 308, 530, 795 [IMAGE AVAILABLE]
10. 5,681,679, Oct. 28, 1997, Overcoated electrophotographic imaging member with resilient charge transport layer; Richard L. Schank, et al., 430/59, 66, 83 [IMAGE AVAILABLE]
11. 5,680,008, Oct. 21, 1997, Compact low-noise dynodes incorporating semiconductor secondary electron emitting materials; George R. Brandes, et al., 313/533, 103CM, 105CM, 534 [IMAGE AVAILABLE]
12. 5,664,032, Sep. 2, 1997, Display panel with electrically-controlled waveguide-routing; William K. Bischel, et al., 385/4, 2, 8, 10, 14, 15, 16, 17, 37, 40, 130, 131, 901 [IMAGE AVAILABLE]
13. 5,652,817, Jul. 29, 1997, Optical power splitter with electrically-controlled switching structures; Michael J. Brinkman, et al., 385/37, 16 [IMAGE AVAILABLE]
14. 5,647,036, Jul. 8, 1997, Projection display with electrically-controlled waveguide routing; David A. G. Deacon, et al., 385/27, 9 [IMAGE AVAILABLE]
15. 5,637,901, Jun. 10, 1997, Integrated circuit with diode-connected transistor for reducing ESD damage; David F. Beigel, et al., 257/355,

16. 5,635,434, Jun. 3, 1997, Ceramic ferroelectric composite material-BSTO-magnesium based compound; Louise Sengupta, 501/138, 120, 121, 135, 136, 137 [IMAGE AVAILABLE]

17. 5,630,004, May 13, 1997, Controllable beam director using poled structure; David A. G. Deacon, et al., 385/129, 9, 10, 37, 40 [IMAGE AVAILABLE]

18. H 1,637, Mar. 4, 1997, Laser-assisted fabrication of bipolar transistors in silicon-on-sapphire (SOS); Bruce W. Offord, et al., 438/311; 148/DIG.11, DIG.92, DIG.150; 438/799 [IMAGE AVAILABLE]

19. 5,591,553, Jan. 7, 1997, Filtered photoreceptor; Christopher Snelling, 430/46, 42 [IMAGE AVAILABLE]

20. 5,587,224, Dec. 24, 1996, Developing apparatus including a coated developer roller; Bing R. Hsieh, et al., 428/195; 399/279, 286; 430/59, 122 [IMAGE AVAILABLE]

21. 5,586,206, Dec. 17, 1996, Optical power splitter with electrically-controlled switching structures; Michael J. Brinkman, et al., 385/37, 8, 16 [IMAGE AVAILABLE]

22. 5,581,642, Dec. 3, 1996, Optical frequency channel selection filter with electronically-controlled grating structures; David A. G. Deacon, et al., 385/15; 359/573; 385/10, 37, 40 [IMAGE AVAILABLE]

23. 5,581,194, Dec. 3, 1996, Method and apparatus for passive optical characterization of semiconductor substrates subjected to high energy (MEV) ion implantation using high-injection surface photovoltaic; John K. Lowell, 324/752 [IMAGE AVAILABLE]

24. 5,571,339, Nov. 5, 1996, Hydrogen passivated heteroepitaxial III-V photovoltaic devices grown on lattice-mismatched substrates, and process; Steven A. Ringel, et al., 136/252, 262; 257/431; 438/94, 933 [IMAGE AVAILABLE]

25. 5,544,268, Aug. 6, 1996, Display panel with electrically-controlled waveguide-routing; William K. Bischel, et al., 385/4, 16 [IMAGE AVAILABLE]

26. 5,541,524, Jul. 30, 1996, Burn-in technologies for unpackaged integrated circuits; David B. Tuckerman, et al., 324/754, 758, 760 [IMAGE AVAILABLE]

27. 5,525,541, Jun. 11, 1996, Method of making an electronic and/or photonic component; Philippe Krauz, et al., 438/38; 148/DIG.72; 438/47, 540, 779, 796, 936 [IMAGE AVAILABLE]

28. 5,504,772, Apr. 2, 1996, Laser with electrically-controlled grating reflector; David A. G. Deacon, et al., 372/102 [IMAGE AVAILABLE]

29. 5,491,762, Feb. 13, 1996, ATM switch with electrically-controlled waveguide-routing; David A. G. Deacon, et al., 385/16, 37 [IMAGE AVAILABLE]

30. 5,488,681, Jan. 30, 1996, Method for controllable optical power splitting; David A. G. Deacon, et al., 385/37 [IMAGE AVAILABLE]

31. 5,446,302, Aug. 29, 1995, Integrated circuit with diode-connected transistor for reducing ESD damage; David F. Beigel, et al., 257/355, 362, 506, 565, 586 [IMAGE AVAILABLE]

32. 5,436,496, Jul. 26, 1995, Vertical fuse device; Rick C. Jerome, et al., 257/529, 539, 570, 751, 768 [IMAGE AVAILABLE]

33. 5,420,081, May 30, 1995, Preparation of fullerene/glass composites; Benjamin R. Mattes, et al., 501/12, 32 [IMAGE AVAILABLE]

34. 5,412,242, May 2, 1995, Semiconductor device with p-n junction based on dopant profile in equilibrium with internal electric field created by this junction; David Cahen, et al., 257/442, 102, 744 [IMAGE AVAILABLE]

35. 5,409,792, Apr. 25, 1995, Photoreceptor containing dissimilar charge transporting small molecule and charge transporting polymer; John F. Yanus, et al., 430/59 [IMAGE AVAILABLE]

36. 5,406,214, Apr. 11, 1995, Method and apparatus for measuring minority carrier lifetime in semiconductor materials; Janos Boda, et al., 324/765, 642, 752 [IMAGE AVAILABLE]

37. 5,395,794, Mar. 7, 1995, Method of treating semiconductor materials; Vladislav E. Sklyarevich, et al., 438/535, 530, 606, 663, 795 [IMAGE AVAILABLE]

38. 5,395,481, Mar. 7, 1995, Method for forming silicon on a glass substrate; Anthony M. McCarthy, 438/479; 117/43; 148/DIG.12, DIG.150; 438/459, 970 [IMAGE AVAILABLE]

39. 5,394,426, Feb. 28, 1995, Diode laser bar assembly; David E. Joslin, 372/50, 36 [IMAGE AVAILABLE]

40. 5,389,792, Feb. 14, 1995, Electron microprobe utilizing thermal detector arrays; Don DiMarzio, et al., 250/370.06, 336.2, 370.01, 370.15 [IMAGE AVAILABLE]

41. 5,386,277, Jan. 31, 1995, Developing apparatus including a coated developer roller; Dah A. Hays, et al., 399/281, 291; 430/58 [IMAGE AVAILABLE]

42. 5,381,434, Jan. 10, 1995, High-temperature, uncooled diode laser; Rajaram Bhat, et al., 372/45 [IMAGE AVAILABLE]

43. 5,332,689, Jul. 26, 1994, Method for depositing low bulk resistivity doped films; Gurtej S. Sandhu, et al., 438/491; 148/DIG.38; 438/925 [IMAGE AVAILABLE]

44. 5,316,793, May 31, 1994, Directed effusive beam atomic layer epitaxy system and method; Robert M. Wallace, et al., 427/248.1; 118/50, 715, 719; 427/255.1, 255.2, 294 [IMAGE AVAILABLE]

45. 5,312,762, May 17, 1994, Method of measuring an analyte by measuring electrical resistance of a polymer film reacting with the analyte; Anthony Guiseppi-Elie, 436/149; 204/403; 435/4, 14, 25, 177, 180, 182, 817; 436/806 [IMAGE AVAILABLE]

46. 5,266,502, Nov. 30, 1993, STM memory medium; Takao Okada, et al., 438/766 [IMAGE AVAILABLE]

47. 5,244,762, Sep. 14, 1993, Electrophotographic imaging member with blocking layer containing uncrosslinked chemically modified copolymer; John W. Spiewak, et al., 430/64, 58 [IMAGE AVAILABLE]

48. 5,212,101, May 18, 1993, Substitutional carbon in silicon; Leigh T. Canham, et al., 438/45; 148/DIG.4, DIG.155; 438/528, 530, 918 [IMAGE AVAILABLE]

49. 5,175,503, Dec. 20, 1992, Ascertaining imaging cycle life of a photoreceptor; Satchi [REDACTED] and Mishra, et al., 324/452, 47 [IMAGE AVAILABLE]

50. 5,173,792, Dec. 22, 1992, Electrooptical display with compensative redundancy means; Yojiro Matsueda, 349/54, 39, 42, 48, 50, 51 [IMAGE AVAILABLE]

51. 5,160,374, Nov. 3, 1992, Process and apparatus for preventing the pulse discharge of insulators in ionizing radiation; Arthur R. Frederickson, et al., 106/401, 287.19, 400, 455; 252/500, 511; 361/212, 220; 428/922, 931 [IMAGE AVAILABLE]

52. 5,157,015, Oct. 20, 1992, Process for preparing superconducting films by radio-frequency generated aerosol-plasma deposition in atmosphere; Robert L. Snyder, et al., 505/401; 427/62, 226, 453, 565; 505/477, 737 [IMAGE AVAILABLE]

53. 5,151,766, Sep. 29, 1992, Semiconductor component; Marcel Huppi, 257/617, 156, 611, 612 [IMAGE AVAILABLE]

54. 5,149,404, Sep. 22, 1992, Fine line scribing of conductive material; Greg E Blonder, et al., 205/656, 686; 216/13, 48, 63, 67; 219/69.11, 69.17 [IMAGE AVAILABLE]

55. 5,143,089, Sep. 1, 1992, Assembly and method of communicating electrical signals between electrical therapeutic systems and body tissue; Eckhard Alt, 607/121; 600/374 [IMAGE AVAILABLE]

56. 5,138,520, Aug. 11, 1992, Methods and apparatus for material deposition; Larry D. McMillan, et al., 361/311; 427/565, 581, 586 [IMAGE AVAILABLE]

57. 5,100,868, Mar. 31, 1992, Process for preparing superconducting films by radio-frequency-generated aerosol plasma deposition; Robert L. Snyder, et al., 505/401; 427/62, 226, 314, 377, 421, 453, 565; 505/477, 730, 737, 742 [IMAGE AVAILABLE]

58. 5,063,538, Nov. 5, 1991, Optoelectronic signal recording medium and method of making same; Manfred R. Kuehnle, 365/106; 396/661; 428/689, 698, 699, 700, 702; 430/60, 84 [IMAGE AVAILABLE]

59. 5,021,843, Jun. 4, 1991, Semiconductor integrated circuit; Tadahiro Ohmi, 257/379, 401 [IMAGE AVAILABLE]

60. 4,914,059, Apr. 3, 1990, Process for the heat flash vapour phase deposition of an insulating layer on a III-V material substrate and its application to the production of a MIS structure; Yves Nissim, et al., 438/590; 427/255.2, 255.3; 438/591, 779, 796 [IMAGE AVAILABLE]

61. 4,907,053, Mar. 6, 1990, Semiconductor integrated circuit; Tadahiro Ohmi, 257/315, 347 [IMAGE AVAILABLE]

62. 4,902,967, Feb. 20, 1990, Scanning electron microscopy by photovoltage contrast imaging; Larry D. Flesner, 324/751; 250/311, 492.2; 324/765 [IMAGE AVAILABLE]

63. 4,862,414, Aug. 29, 1989, Optoelectronic recording tape or strip comprising photoconductive layer on thin, monocrystalline, flexible sapphire base; Manfred R. Kuehnle, 365/106; 396/661; 428/689, 698, 699, 700, 702; 430/84 [IMAGE AVAILABLE]

64. 4,862,238, Aug. 29, 1989, Transistors; John M. Shannon, 257/29, 475, 497, 498 [IMAGE AVAILABLE]

65. 4,839,588, Jun. 1989, Method for the examination of electrically active impurities of semiconductor material or structures and measuring arrangement for carrying out the method; Wolfgang Jantsch, et al., 324/766, 636, 639, 642, 719 [IMAGE AVAILABLE]

66. 4,797,721, Jan. 10, 1989, Radiation hardened semiconductor device and method of making the same; Sheng T. Hsu, 257/354, 429 [IMAGE AVAILABLE]

67. 4,732,866, Mar. 22, 1988, Method for producing low noise, high grade constant semiconductor junctions; Jerry L. Chruma, et al., 438/530; 257/606; 438/795 [IMAGE AVAILABLE]

68. 4,670,063, Jun. 2, 1987, Semiconductor processing technique with differentially fluxed radiation at incremental thicknesses; Steven R. Schachameyer, et al., 117/103, 904; 148/DIG.93; 427/582; 438/487 [IMAGE AVAILABLE]

69. 4,555,273, Nov. 26, 1985, Furnace transient anneal process; David A. Collins, et al., 438/522; 118/500, 641, 724, 728; 148/DIG.3, DIG.6, DIG.71, DIG.76; 219/385, 390; 432/11, 45, 148, 198; 438/796 [IMAGE AVAILABLE]

70. 4,523,370, Jun. 18, 1985, Process for fabricating a bipolar transistor with a thin base and an abrupt base-collector junction; Paul A. Sullivan, et al., 438/365; 148/DIG.11, DIG.92; 257/56; 438/348, 363 [IMAGE AVAILABLE]

71. 4,522,657, Jun. 11, 1985, Low temperature process for annealing shallow implanted N+/P junctions; Ajeet Rohatgi, et al., 438/57; 257/461; 438/528 [IMAGE AVAILABLE]

72. 4,490,709, Dec. 25, 1984, InP:Fe Photoconducting device; Robert B. Hammond, et al., 338/15; 257/459, 629, 744 [IMAGE AVAILABLE]

73. 4,462,150, Jul. 31, 1984, Method of forming energy beam activated conductive regions between circuit elements; Hidetaro Nishimura, et al., 438/128; 148/DIG.91, DIG.92; 257/538; 427/523, 555; 438/131, 934 [IMAGE AVAILABLE]

✓ 74. 4,452,644, Jun. 5, 1984, Process for **doping** semiconductors; Michel Bruel, et al., 438/536; 250/492.1; 257/655 [IMAGE AVAILABLE]

75. 4,437,969, Mar. 20, 1984, Offset-gate chemical-sensitive field-effect transistors (OG-CHEMFETS) with electrolytically-programmable selectivity; Arthur K. Covington, et al., 204/403, 415, 416, 420; 257/253, 414, 665; 435/817 [IMAGE AVAILABLE]

76. 4,436,557, Mar. 13, 1984, Modified laser-annealing process for improving the quality of electrical P-N junctions and devices; Richard F. Wood, et al., 438/89; 136/258, 261; 148/DIG.90, DIG.92, DIG.93; 257/75, 104, 655; 438/535, 537, 799 [IMAGE AVAILABLE]

77. 4,400,715, Aug. 23, 1983, Thin film semiconductor device and method for manufacture; Steven G. Barbee, et al., 257/74, 477, 520 [IMAGE AVAILABLE]

78. 4,380,864, Apr. 26, 1983, Method for providing in-situ non-destructive monitoring of semiconductors during laser annealing process; Pankaj K. Das, 438/17; 148/DIG.91, DIG.93; 310/313R; 324/703, 719; 364/821 [IMAGE AVAILABLE]

79. 4,379,727, Apr. 12, 1983, Method of laser annealing of subsurface ion implanted regions; Howard H. Hansen, et al., 438/530; 148/DIG.92, DIG.93; 427/523, 555; 438/369, 795 [IMAGE AVAILABLE]

80. 4,370,176, Jan. 11, 1983, Process for fast dropping of semiconductors; Michel Bruel, 438/514; 250/492.2; 257/617; 438/515, 535 [IMAGE AVAILABLE]

✓ 81. 4,368,083, Jan. 11, 1983, Process for **doping** semiconductors; Michel Bruel, et al., 438/536; 257/607, 617, 655 [IMAGE AVAILABLE]

82. 4,329,209, May 11, 1982, Process using an oxidant depolarized solid polymer electrolyte chlor-alkali cell; Harlan B. Johnson, 205/512; 204/222, 273; 205/511, 525 [IMAGE AVAILABLE]

83. 4,317,844, Mar. 2, 1982, Semiconductor device having a body of amorphous silicon and method of making the same; David E. Carlson, 438/92; 118/50.1, 723E, 723ER; 204/164; 427/578; 438/96, 485 [IMAGE AVAILABLE]

84. 4,273,950, Jun. 16, 1981, Solar cell and fabrication thereof using microwaves; Sanjiv R. Chitre, 136/255, 256, 258, 261; 148/DIG.153; 219/690; 257/448; 427/545, 557; 438/97, 530, 558 [IMAGE AVAILABLE]

85. 4,266,986, May 12, 1981, Passivation of defects in laser annealed semiconductors; Janet L. Benton, et al., 438/475; 148/DIG.24, DIG.90, DIG.93; 257/651; 372/44; 427/569, 596; 438/798 [IMAGE AVAILABLE]

86. 4,240,843, Dec. 23, 1980, Forming self-guarded p-n junctions by epitaxial regrowth of amorphous regions using selective radiation annealing; George K. Celler, et al., 438/530; 117/8; 148/DIG.55, DIG.92, DIG.93; 219/121.6; 257/523; 438/414, 799 [IMAGE AVAILABLE]

87. 4,234,356, Nov. 18, 1980, Dual wavelength optical annealing of materials; David H. Auston, et al., 438/799; 117/54, 904, 934, 936; 148/DIG.3, DIG.90, DIG.93; 219/121.6, 121.66; 250/492.2; 257/617; 438/530, 796 [IMAGE AVAILABLE]

88. 4,214,918, Jul. 29, 1980, Method of forming polycrystalline semiconductor interconnections, resistors and contacts by applying radiation beam; Arnon Gat, et al., 438/618; 148/DIG.93; 219/121.6; 257/66, 379, 412; 427/492, 552, 586; 438/585, 659, 660, 663 [IMAGE AVAILABLE]

89. 4,198,246, Apr. 15, 1980, **Pulsed** laser irradiation for reducing resistivity of a **doped** polycrystalline silicon film; Chung P. Wu, 428/446; 136/258; 148/DIG.93; 219/121.6; 257/75, 754; 427/554; 438/795, 799, 934 [IMAGE AVAILABLE]

90. 4,181,538, Jan. 1, 1980, Method for making defect-free zone by laser-annealing of **doped** silicon; Jagdish Narayan, et al., 438/473; 136/261; 148/DIG.3, DIG.90, DIG.92, DIG.93, DIG.97; 219/121.6, 121.66; 257/607, 655; 438/530, 799 [IMAGE AVAILABLE]

✓ 91. 4,147,563, Apr. 3, 1979, Method for forming p-n junctions and solar-cells by laser-beam processing; Jagdish Narayan, et al., 438/89; 136/261; 148/DIG.90, DIG.92, DIG.153; 219/121.85; 257/464; 438/535 [IMAGE AVAILABLE]

92. 4,131,484, Dec. 26, 1978, Frequency adjusting a piezoelectric device by lasering; Robert D. Caruso, et al., 134/1; 29/25.35, 593; 219/121.85; 310/312 [IMAGE AVAILABLE]

93. 4,109,029, Aug. 22, 1978, High resolution electron beam microfabrication process for fabricating small geometry semiconductor devices; Faik S. Ozdemir, et al., 438/14; 250/492.2; 427/8, 96, 383.1; 430/296, 319; 438/571, 949, 975 [IMAGE AVAILABLE]

94. 4,081,794, Mar. 1978, Alloy junction archival memory plane and methods for writing on and thereon; Harold G. Parks, et al., 365/118; 219/121.16, 121.17, 121.29, 121.61, 121.85; 257/428, 917; 365/103, 114; 438/128, 537, 798 [IMAGE AVAILABLE]

95. 4,064,521, Dec. 20, 1977, Semiconductor device having a body of amorphous silicon; David Emil Carlson, 257/54; 136/255, 258; 257/458, 461; 427/255.1, 578 [IMAGE AVAILABLE]

96. 3,872,314, Mar. 18, 1975, Electroluminescent devices and apparatus including such devices; Anthony Ralph Peaker, et al., 250/552, 553; 313/500 [IMAGE AVAILABLE]

97. 3,772,874, Nov. 20, 1973, DISPLAY APPARATUS AND CHRONOMETER UTILIZING OPTICALLY VARIABLE LIQUID; Issai Lefkowitz, 368/242; 345/51; 349/33, 141, 142; 968/941, 950, DIG.1 [IMAGE AVAILABLE]

98. 3,666,960, May 30, 1972, REVERSE BIAS PULSING OF JUNCTION DIODES TO REDUCE DETERIORATION; Robert William Dawson, 327/514; 313/499; 327/530 [IMAGE AVAILABLE]

99. 3,657,617, Apr. 18, 1972, POINT CONTACT SEMICONDUCTOR DEVICE; Cyril Morgan, 257/41 [IMAGE AVAILABLE]

100. 3,620,851, Nov. 16, 1971, METHOD FOR MAKING A BURIED LAYER SEMICONDUCTOR DEVICE; William J. King, et al., 438/526; 257/429; 438/56, 370 [IMAGE AVAILABLE]

101. 3,609,478, Sep. 28, 1971, BURIED-LAYER SEMICONDUCTOR DEVICE FOR DETECTING AND MEASURING THE ENERGY AND ATOMIC NUMBER OF IMPINGING ATOMIC PARTICLES; William J. King, et al., 257/430; 250/370.01, 370.02, 370.14; 257/465 [IMAGE AVAILABLE]